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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/389,321	09/03/99	HIRAMOTO T	026350-028

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EXAMINER	
DICKEY, T	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 10/19/01

#11

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/389,321	Applicant(s) HIRAMOTO ET AL.	
	Examiner Thomas L Dickey	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 08/07/01 has been entered.

Drawings

2. The drawings are objected to by the PTO Draftsperson for the reasons noted on the Notice of Draftsperson's Patent Drawing Review, form PTO-948, attached to paper #7, mailed 02/09/01.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Applicant's specification makes the following definitions:

1. Of the terms applicant uses, it is found that MOS and DTMOS are terms used fairly often by those skilled in the art, where it is understood that a MOS has a gate, oxide or similar gate insulator, source, drain, and channel region, while a DTMOS in

addition has an electrical connection between the gate and the channel region. Application at p. 2 ll. 12-24.

2. EIB, electrically induced body, and EIB-MOS, are terms for which no reference can be found outside of applicant's own work. Outside of the current application, these terms appear only in English abstract of JP 2000260991 A, which is the laid-open copy of applicant's priority document. EIB, electrically induced body, and EIB-MOS all appear to refer to an SOI MOS adapted for biasing the voltage of the substrate relative to the body, i.e. channel region. Application at p. 9, ll. 7-11. For brevity, the examiner has adopted this terminology and the examiner has coined, in addition, the term EIB-FET, to refer to any FET, either MOS or junction, which is adapted for biasing the voltage of the substrate relative to the body.
3. VTMOS is an EIB-MOS where the substrate voltage bias may be switched from a first voltage to a second, lower bias. Application at p. 2, ll 7-11.
4. Accumulation mode means a FET with its channel having the same conductivity as its drain and source.

A. Claims 1, 2, 4-6, 7,8, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over BURR et al. (6,100,567).

With regard to claims 1,5,7, and 11, Burr discloses a complementary FET (field effect transistor) comprising an SOI (502, 504) which includes a substrate (552, 554) composed of a semi-conducting material, a single crystal semi-conducting layer (512, 514, 516 or 520, 522,524), an insulating oxide substrate (508) where the semi-

conducting layer (512, 514, 516), is made of a source (512, 520), drain (514, 522), and a surrounded region (516, 524) that is surrounded by the source (512, 520) and the drain (514, 522). Burr further discloses a connection (544, 546) that adapts the substrate (540, 542) to be applied with a voltage of a first polarity, and a depletion region, i.e. a depletion layer (328). Note figs. 3, 5, and col. 1, l. 27.

Burr does not teach an MOS because Burr does not explicitly show a metal gate, or an oxide insulating that gate from the surrounded region. Rather Burr teaches a conductive polysilicon layer that functions as a gate, with no particular means specified for achieving the gate. Further, Burr does not teach a composition surface in the depletion layer that is in contact with the insulating layer and in which charges of a second polarity are induced.

However, the poly gate of Burr is recognized as the equivalent of a metal gate. Further, it would be clear that an insulator could be placed between the transistor body and Burr's gate to form an FET of the MOS type. In context, the "composition surface" is the depletion layer surface in contact with the insulating layer. One skilled in the art would understand that applying a voltage to the conductive substrate would cause all surfaces, including the one opposing the composition surface, to have that voltage. One skilled in the art would further understand that when placed in opposition to a surface having voltage of first polarity, the surface of a conductive body such as the depletion layer would carry charges of second polarity. Therefore, it would be obvious to one of ordinary skill the art to build an FET of the MOS type according to the teachings of Burr,

in order to obtain the advantages of an FET with variable threshold voltage taught by Burr. It would be obvious that that FET would include a composition surface in the depletion layer in contact with the insulating layer in which charges of a second polarity are induced.

With regard to claims 2 and 8, Burr teaches an DT-FET where the undepleted channel region is electrically connected to the gate. With an oxide layer between gate and channel, this FET would be a DTMOS transistor. See fig. 2, esp. part 230. It would have been obvious to one of ordinary skill in the art to combine Burr's DT-FET with Burr's EIB-FET and place an insulator between the transistor body and Burr's gate to form an DT-FET of the MOS type in order to combine the voltage threshold reduction realized by the DT-FET, as taught by Burr, with the variable threshold voltage advantages of the EIB-FET, as taught by Burr.

With regard to claims 4 and 10, applicant defines VTMOS as a transistor in which the threshold voltage is controlled by "(the) whole of a chip" in which the VTMOS transistor is provided, or alternatively, as a transistor where a first voltage is applied to the substrate in the "active mode," and a second, smaller, voltage is applied in the "standby mode." Application, page 2, lines 8-11.

It should be reiterated that applicant is the first and only user of the term "VTMOS." This term, as a claim term, must therefore be read as defined in the specification. Using applicant's second definition, a VTMOS is a transistor where a first voltage is applied to the substrate and (alternatively) a second, smaller, voltage is

applied. A VTMOS, so defined, would have been obvious to one of ordinary skill in the art under the same analysis used for the EIB-MOS.

With regard to claims 6 and 12, Burr teaches the step of applying a voltage of a first polarity to the substrate of an EIB-FET, and that this step controls the threshold voltage. See Burr, col. 6 table 1. For this reason, it would have been obvious to one of ordinary skill in the art to perform the same step with a EIB-MOS which includes a semiconducting substrate, a semiconducting single crystal layer, an insulating oxide interposed between, source, drain and surround regions, depletion layer and composition surface, in order to tune the performance of the FET, as taught by Burr.

B. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of WARASHINA, et al. (5,698,885)

Burr discloses an EIB-FET with all the limitations of claim 3 except the MOS gate structure, composition surface, induced charges of second polarity, and accumulation mode, i.e. channel having same conductivity as introduced carriers. Warashina et al. discloses a MOS FET in accumulation mode. The MOS FET is known to reduce power by limiting gate current. Accumulation mode is described by Warashina et al. as reducing power by reducing threshold voltage. Burr describes the EIB-FET as reducing power by reducing threshold voltage. Therefore, it would have been obvious to one of ordinary skill in the art to combine the MOS-FET of Warashina et al. with the EIB-FET of Burr, in order to reduce power consumption.

Response to Arguments

5. Applicant's arguments filed 02/16/00 have been fully considered but they are not persuasive.

It is argued, at page 7 of the remarks, that "Claims 1 and 6 claim a MOS transistor and a method of controlling the threshold voltage of a MOS by applying a voltage of first polarity to a substrate." Burr '567 discloses a transistor and a method of controlling the threshold voltage of a MOS by applying a voltage of first polarity to a substrate, and this fact was pointed out in applicant's first rejection. Further, it was argued that it would have been obvious to substitute a MOS transistor for Burr's transistor. Applicant has neither denied this fact nor refuted this argument.

In response to applicant's argument that applicant intends for this structure to "induc[e] charges of a second polarity over a composition surface of a surrounded region [and] ... operat[e] a circuit at high speed while reducing power consumption," a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

It is further argued at page 7 that an EIB is used for "accumulating or inverting the interface between the SOI and the buried oxide." Applicant is the sole user of the term "EIB" in this context and is free to define this term as he likes. The response, once again, is that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

It is argued, on page 8 of the response, that "a VT-MOS is a *conventional* EIB-MOS." Both "VT-MOS" and "EIB-MOS" are terms applicant has made up to describe his invention and applicant is free to make this disinction.

It is argued, on page 9 of the application, that "Burr merely discloses a device having a depletion region 328 that extends completely down to the oxide layer 308."

In response to applicant's argument that the in disclosing a fully depleted MOSFET Burr differentiates itself from certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a body effect γ which is lower than that found in a fully depleted MOSFET) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the

specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Also on page 9, applicant argues that Burr fails to show "a composition surface in the depletion region in contact with the insulating layer in which charges of second polarity are induced." These charges are in fact an obvious, or even inherent, result of the impressing of a voltage of first polarity on the substrate, as Burr recites. Note figure 5 of Burr.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Papers related to this application may be submitted to Technology Center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 3-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2826 Fax Center number is (703) 308-7722 and 308-7724. The Group 2800 Fax Center is to be used only for papers related to Group 2800 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to Thomas Dickey whose telephone number is **(703) 308-0980**. The Examiner is in the Office generally between the hours of 8:00 AM to 5:00 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**.

TLD
02/2001

Minh Loan Tran

Minh Loan Tran
Primary Examiner